

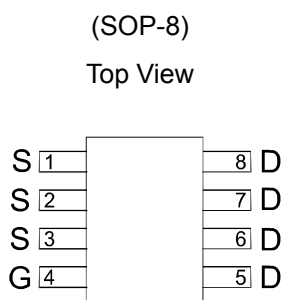
P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME9435A is the P-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and lower power loss that are needed in a very small outline surface mount package.

PIN CONFIGURATION

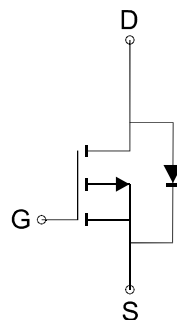


FEATURES

- $R_{DS(ON)} \leq 40m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 60m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



P-Channel MOSFET

Ordering Information: ME9435A (Pb-free)

ME9435A-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A = 25^\circ C$	-6.3
		$T_A = 70^\circ C$	-5
Pulsed Drain Current ¹⁾	I_{DM}	-25	A
Maximum Power Dissipation	P_D	$T_A = 25^\circ C$	2.5
		$T_A = 70^\circ C$	1.6
Operating Junction Temperature	T_J	-55 to 150	°C
Junction-to-Ambient Thermal Resistance*	$R_{\theta JA}$	50	°C/W

*The device mounted on 1in2 FR4 board with 2 oz copper



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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1.0		-3.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24 V, V _{GS} =0V			-1	μA
R _{DS(on)}	Drain-Source On-State Resistance ^a	V _{GS} =-10V, I _D = -5.3A		31	40	mΩ
		V _{GS} =-4.5V, I _D = -4.2A		40	60	
DYNAMIC						
R _g	Gate resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		5.5		Ω
C _{iss}	Input capacitance	V _{DS} =-15V, V _{GS} =0V, f=1.0MHz		840	960	pF
C _{oss}	Output Capacitance			120		
C _{rss}	Reverse Transfer Capacitance			35		
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-5.3A		21	25	nC
Q _{gs}	Gate-Source Charge			6		
Q _{gd}	Gate-Drain Charge			5.4		
t _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, R _L =15Ω I _D =-1A, V _{GEN} =-10V R _G =6Ω		32	40	ns
t _r	Turn-On Rise Time			13	16	
t _{d(off)}	Turn-Off Delay Time			58	75	
t _f	Turn-Off Fall Time			6	9	

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

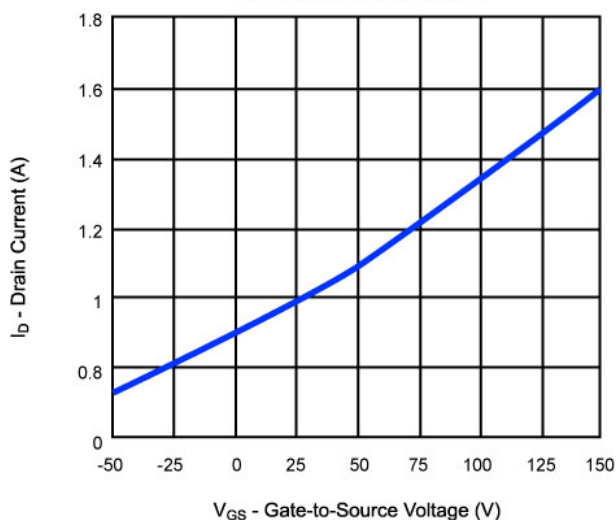
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



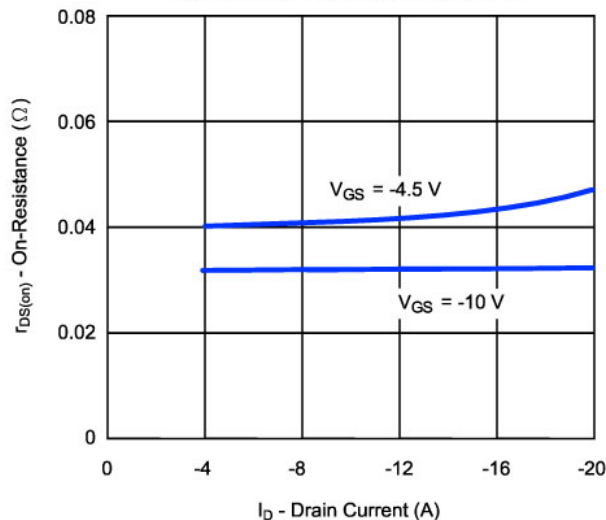
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Typical Characteristics (T_J = 25°C Noted)

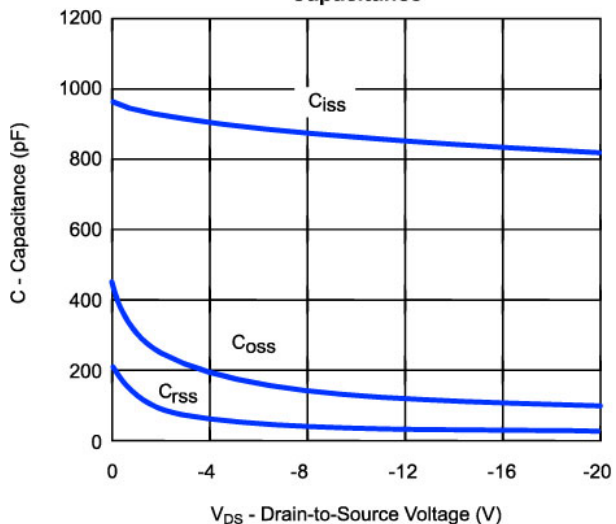
Transfer Characteristics



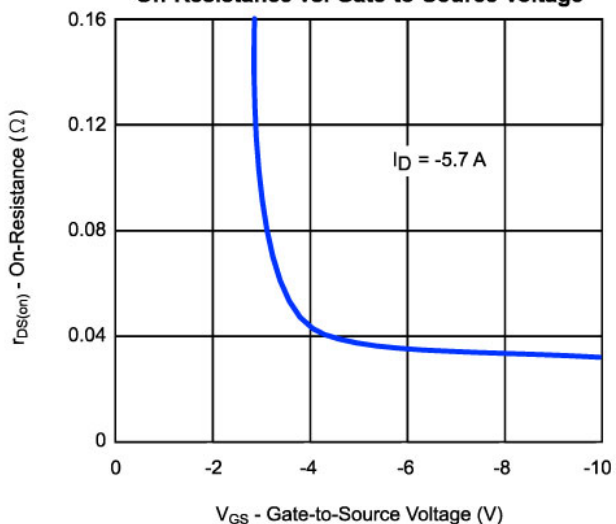
On-Resistance vs. Drain Current



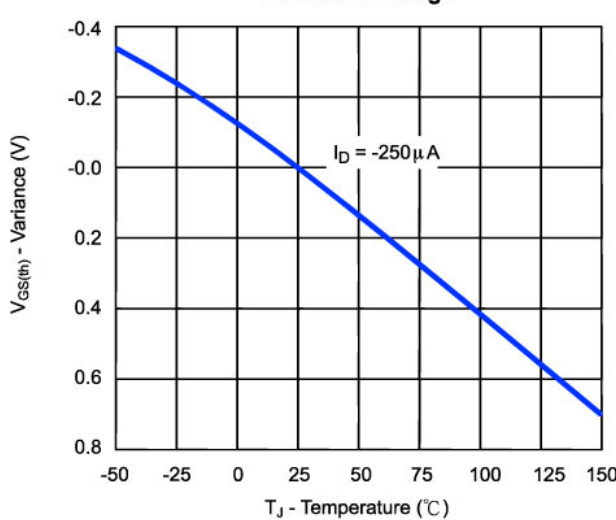
Capacitance



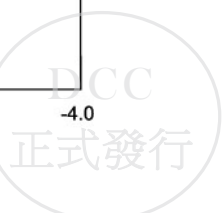
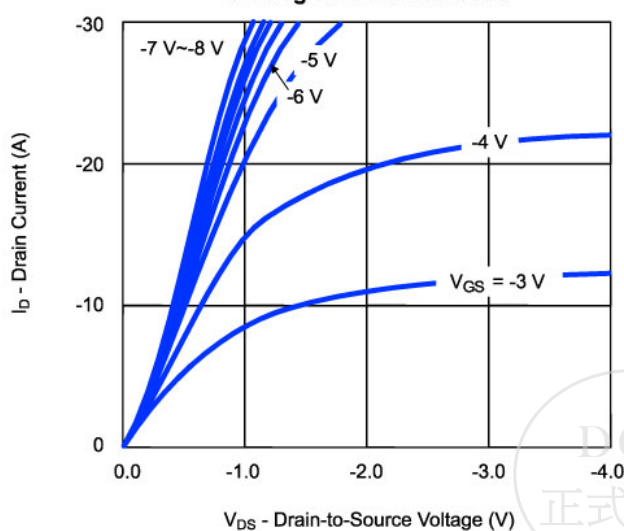
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

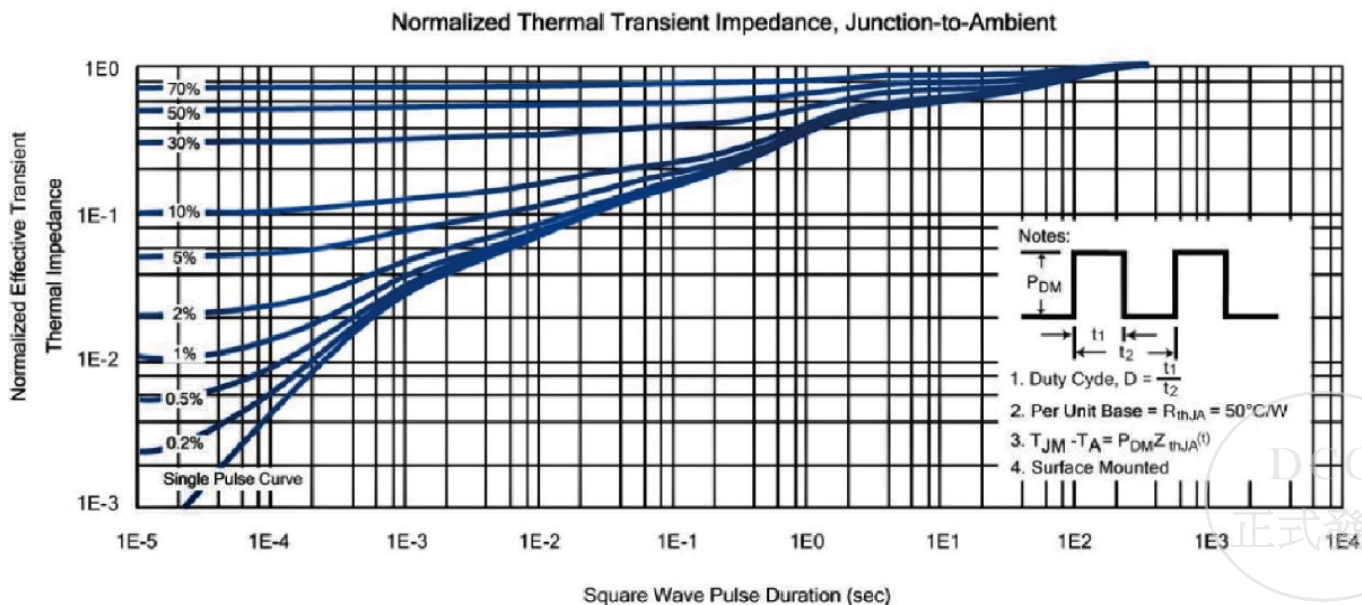
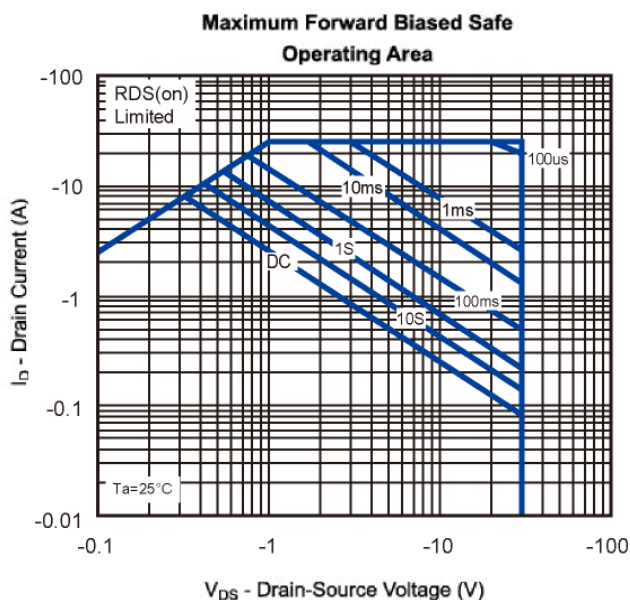
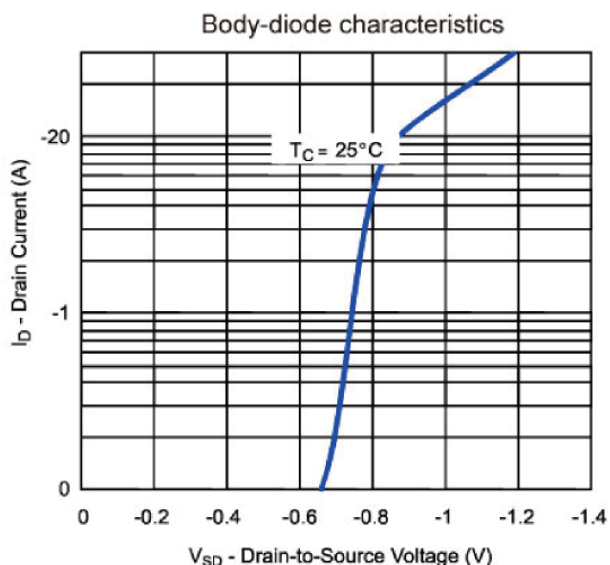
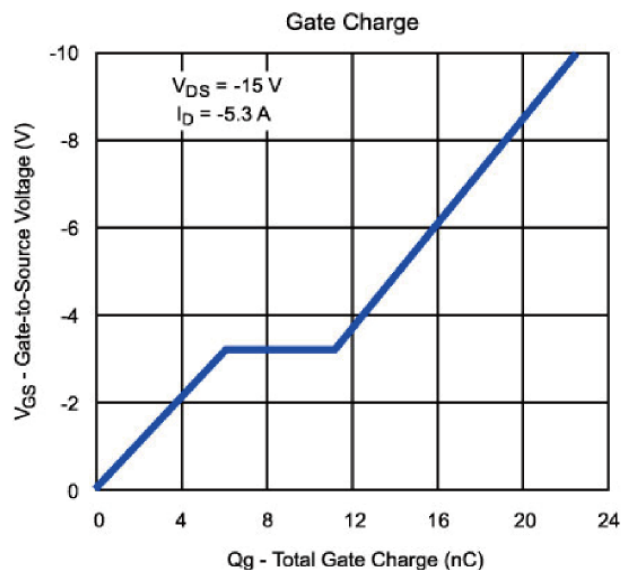


On-Region Characteristics

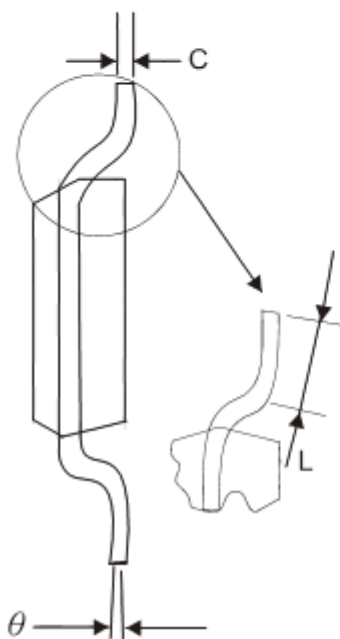
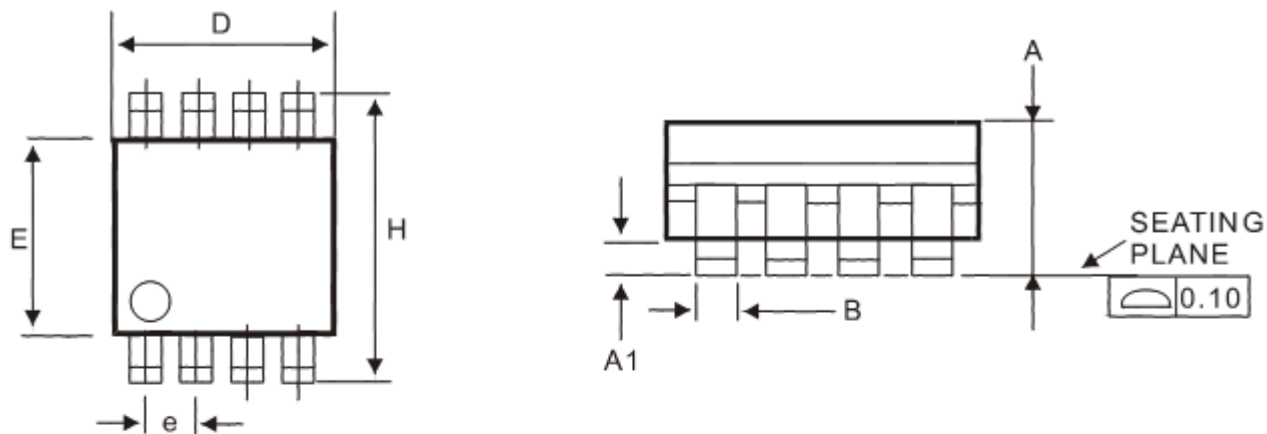


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Typical Characteristics (T_J = 25°C Noted)



SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

